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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,606	03/01/2004	Jiong-Ping Lu	TI 37479	9593

23494 7590 06/13/2005

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
TRAN, LONG K	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/790,606	LU, JIONG-PING	
	Examiner	Art Unit	
	Long K. Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Response to Restrict. on April 15, 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10 - 19* is/are pending in the application.

4a) Of the above claim(s) *17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10 – 16, 18 and 19* is/are rejected.

7)☒ Claim(s) *11-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/01/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Group II, claims **10 – 19** without traverse in the reply filed on December22, 2004 is acknowledged; and

Applicant's election of embodiment 2, claims **10 – 16, 18** and **19** in the reply filed on April 15, 2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

2. Claims **1 – 9** and **17** withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected group and species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on December 22, 2004 and April 15, 2005.

Information Disclosure Statement

3. This office acknowledges of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on March 01, 2004.

The references cited on the PTO -1449 form have been considered.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

5. Each of claims **11, 12** and **13** recites a "blanket", which by definition, anything that covers. For examination purposes, a layer cover the underlying layer is considered to be a blanket.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claim **10, 11** and **13** are rejected under 35 U.S.C. 102(e) as being anticipated by Cabral et al. (US Patent Application Publication no. 2005/0064636).

8. Regarding claim **10**, Cabral discloses a method for manufacturing a semiconductor device, comprising:

placing a gate oxide 202 (figure 2A; [0021] lines 3 and 4) over a substrate 200 (figure 2A); and

forming a silicided gate electrode 214 (figure 2E; [0026]) over said gate oxide 202, said silicided gate electrode including a first metal and a second metal (from metal layer 208 (figure 2D; ([0025] lines 5 and 6 and [0026])).

Regarding claim **11**, Cabral discloses depositing a blanket of polysilycon material 204 (figure 2B; [0021], lines 2 and 3) over a blanket of gate oxide 202 (figure 2B),

depositing a blanket of a cobalt-nickel bilayer or a blanket layer of cobalt-nickel alloy 208 (figure 2D; [0025] lines 4 – 10) over the blanket layer of polysilicon material 204 (figure 2D), and annealing the layers to form a blanket of silicided gate electrode material 214 (figure 2E; [0026] and [0027]) including cobalt and nickel.

Regarding claim **13**, Cabral discloses implanting a dopant 206 (figure 2B) into said blanket layer of polysilicon material 204 (figure 2B) to tune a work function of said silicided gate electrode 214 (figure 2E; [0022]; especially, "ion implantation process that uses an ion beam 206 comprising a controlled amount...").

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims **12** and **14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Cabral et al. (US Patent Application Publication no. 2005/0064636) in view of Thakur (US. Patent no. 6,028,002).

Regarding claim **12**, Cabral discloses the claimed invention of claims 10 and 11 except for patterning said blanket layer of silicided gate electrode material to form a silicided gate electrode.

However, Thakur shows a silicided stacked gate electrode comprising layers 22, 23, 24 (metal silicide), and 25 being patterned and etched to form metal silicided gate electrode 31 (figure 3; column 3, lines 38 – 40).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide a step of patterning a blanket layer of silicided gate electrode material as shown by Thakur for patterning the blanket layer of silicided gate electrode material of Cabral, in order to complete the process of forming the transistor gate (column 4, lines 29 – 31).

Regarding claim **14**, Cabral discloses the claimed invention of claims 10, 11 and 13 except for forming a capping layer over said cobalt-nickel bilayer or cobalt-nickel alloy, said capping layer configured to affect a doping profile of said dopant.

However, Thakur shows forming capping layer 25 over the stacked structure of a silicided layer 24 (figure 2) and a conformal, conductively-doped, polysilicon layer 23 (figure 2; column 2, lines 35 – 42). to improve the profile of a refractory metal silicide structure (including conductively-doped polysilicon layer) during the thermal processing (column 4, lines 9 – 19), patterning and etching processes (column 3, lines 60 – 67).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to adding method for manufacturing a semiconductor device of Cabral with a step of forming a capping layer as taught by Thakur, in order to improve the profile of a refractory metal silicide structure (including conductively-doped polysilicon layer) during the thermal processing (column 4, lines 9 – 19), patterning, etching processes (column 3, lines 60 – 67) and a variety of manufacturing processes .

11. Claims **15** and **16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Cabral et al. (US Patent Application Publication no. 2005/0064636) in view of

Thakur (US. Patent no. 6,028,002) further in view of Chang et al. (US Patent Application Publication no. 2004/0262649).

Regarding claim **15**, Cabral and Thakur disclose the claimed invention of claims 10, 11, 13 and 14 except for the capping layer comprises a transition metal-nitride.

However, Chang shows a cap layer 50 (figure 1D) of TiN (a transition metal-nitride, which is known material in the art of making semiconductor devices as a material for forming a capping layer) formed over a blanket of nickel layer 30 (figure 1D; [0026]) and a blanket of cobalt layer 40 (figure 1D).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide the capping layer of Cabral and Thakur with a capping layer comprising a transition metal-nitride as shown by Chang, since it has been held to be within the general skill of worker in the art to select a known material on a basis of its suitability for specific applications.

Regarding claim **16**, Cabral discloses the claimed invention of claims 10 and 11 but fails to disclose a ratio of a thickness of the cobalt layer to a thickness of the nickel layer ranges from about 9:1 to about 2:3 as cited in the present claim.

However, Chang shows layer 40 (figure 1C) of cobalt having thickness of about 2 and 20 nanometers and layer 30 (figure 1C) of nickel having thickness of about 10 and 20 nanometers ([0024]) and [0025]).

It would have been well known in the art of making semiconductor devices to form the workable or optimal range for the ratio of thickness of the cobalt layer to a thickness of the nickel layer ranges from about 9:1 to about 2:3 through routine design of experimentation (DOE) and optimization to obtain optimal device performance. In addition, the applicant has stated in the application description, [0027] lines 9 and 10 that "the ratio may vary depending on the application".

12. Claims **18** and **19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Cabral et al. (US Patent Application Publication no. 2005/0064636) in view of Ku et al. (US Patent Application Publication no. 2004/0266182).

Regarding claim **18**, Cabral discloses the claimed invention of claims 10 and 11 but fails to disclose a ratio of an atomic percent of the cobalt to a thickness of the nickel in the silicided gate ranges from about 9:1 to about 2:3 as cited in the present claim.

Ku shows an alloying metal used in conjunction with a primary nickel component is cobalt ([0017]) and is about 10 atomic percent of the nickel alloy.

It would have been well known in the art of making semiconductor devices to form the workable or optimal range for a ratio of an atomic percent of the cobalt to a thickness of the nickel in the silicided gate ranges from about 9:1 to about 2:3 through routine design of experimentation (DOE) and optimization to obtain optimal device performance. In addition, the applicant has stated in the application description, [0027] lines 9 and 10, that "the ratio may vary depending on the application".

Regarding claim **19**, Cabral discloses the claimed invention of claim 10 and source/drain regions 216 (figure 2D; [0025]) on the substrate but fails to disclose forming source/drain regions in the substrate and forming silicided source/drain regions in the source/drain regions subsequent to forming the silicided gate electrode.

However, Ku shows forming source/drain regions 28 (figure 2B; [0037]) in the substrate 10 (figure 2B) and forming silicided source/drain contact regions (34D; [0038]) to provide metal patterns for connecting the individual transistors to the remainder of the device circuitry ([0039]).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to adding method for manufacturing a semiconductor device of Cabral with a step of forming source/drain regions in the substrate and forming silicided source/drain regions in the source/drain regions subsequent to forming the silicided gate electrode as taught by Ku, in order to provide metal patterns for connecting the individual transistors to the remainder of the device circuitry ([0039]).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 571-272-1797. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LKT

June 2, 2005